After Sales Technical Documentation
RAE/RAK–1N Series

Chapter 2

–Transceiver GE8/GE9–
Baseband Block

Original, 08/96

CONTENTS –Baseband

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Introduction

The baseband engine consists of two multi chip modules (MCM) mounted along with other baseband circuitry and RF parts on a single multilayer PCB. The chassis of the radio unit has separating walls between baseband and RF. All components are surface mounted. Transceiver GE8 is GSM; Tranceiver GE9 is PCN

The connection to the NOKIA 9000 communicator PDA module is made using a board to board connector. The connections to the User Interface module (UIF) are made through the ‘passive’ PDA module. Besides the PDA board to board connector only the SIM/audio and battery connector are on the baseband module. There is no physical connector between the RF and baseband sections.

Technical Summary

Because of extreme size constraints on this product new production technology will be used. Most of the baseband ICs will be integrated in two multi chip modules. These MCMs and all other baseband circuits are mounted on a single multilayer printed circuit board. This board contains also RF parts. The chassis of the radio unit has separating walls between baseband and RF. All components of the baseband section including the MCMs are surface mountable. They are soldered using reflow. The connection to Responder PDA module is made using a board to board connector. The connections to the User Interface module (UIF) are made through the PDA module. Besides the PDA board to board connector only the SIM/audio connector and battery connector are on the baseband module. There is no physical connector between the RF and baseband sections.

Table 1. List of Functional Submodules

Name of submodule	Function
CTRLU	Control Unit for phone
PWRU	Power supply and charging electronics
DSPU	Digital Signal Processing block
AUDIO	Analog audio processing and PCM encoding/decoding
ASIC	D2CA GSM/PCN system specific ASIC; several functions
RFI	RF – baseband interface (analog signals)

The above blocks are only functional blocks and therefore have no type or material codes. Physically the baseband contains two submodules, MCM1 and MCM2 which utilise COB (chip on board) packaging technology. The MCM 1 contains the 7 ICs in the CTRLU submodule plus bypass capacitors and some resistors.

The MCM 2 contains the 6 ICs in DSPU, AUDIO, ASIC and RFI submodules plus bypass capacitors and some resistors. The PWRU module is laid out in the CMT board using conventional SMD assembly. The rest of the functional modules are partly packaged in the MCM's and partly SMD assembled on the CMT board. In the latter description of the modules the functional partitioning will be used.

Table 2. List of Physical Submodules

Name of submodule	Function
MCM1	Contains MCU, SCL, 2xFLASH, 2xSRAM and EEPROM
MCM2	Contains DSP, 2xSRAM, ASIC, RFI and CODEC

Interconnection Diagram

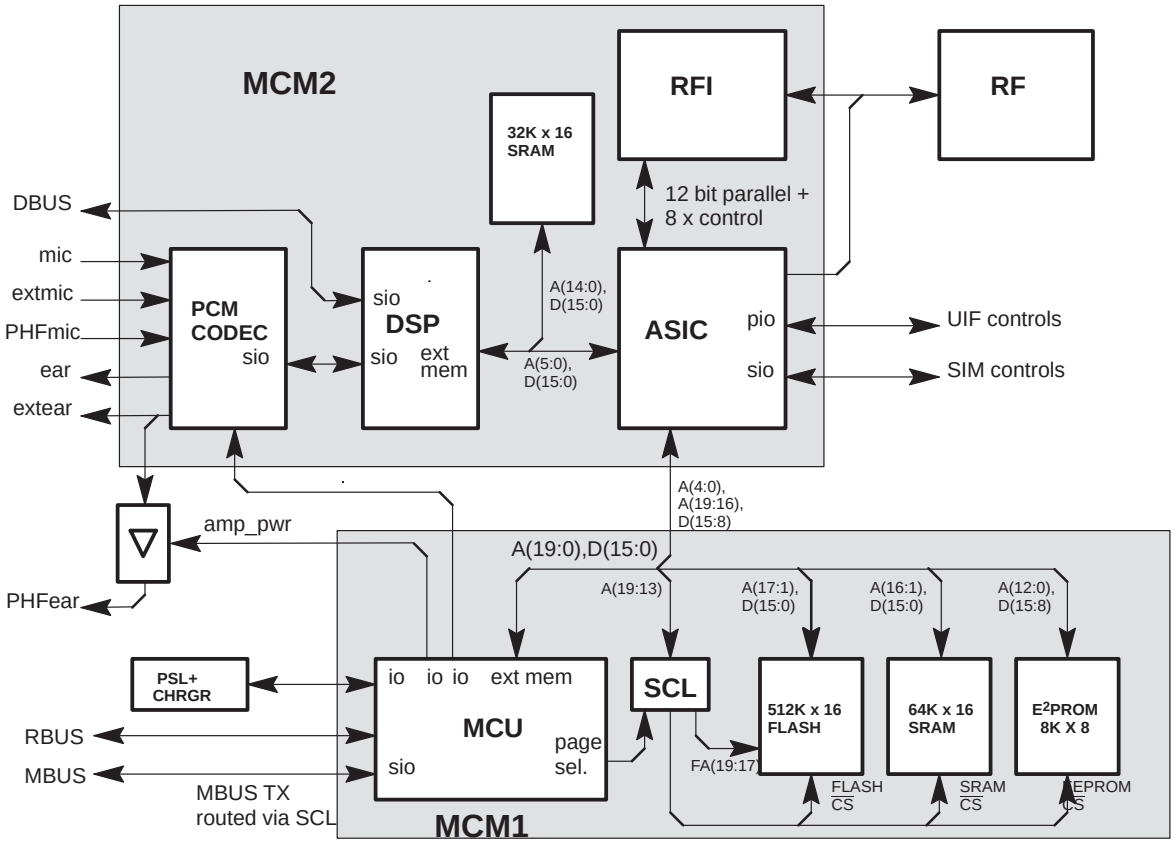

Figure 1. Interconnection diagram

Modes of Operation

There are four different operation modes

– active mode
– idle mode
– acting dead mode
– power off mode

Active Mode

In the active state all circuits are powered and part of the module may be in idle mode.

Idle Mode

The module is usually in the idle mode when there is no call and the phone is in SERV. In the idle mode circuits are reset, powered down and clocks are stopped or the frequency reduced. All the clocks except the main clock from VCXO can be stopped in that mode. Whether the SIM clock is stopped or not depends on the network.

Acting Dead Mode

The acting dead mode means that the baseband is powered but there is no difference from the power off mode from the user point of view. The acting dead mode is used for performing some necessary control functions such as battery voltage measurement and reporting to PDA module.

Power Off Mode

In power off mode only the circuits needed for power up are powered. This means that only power up block inside the PSL+ is powered. The power key is pulled up with a pull up resistor inside the PSL+.

Performance Specifications

DC Characteristics

Table 3. Supply Voltages and Power Consumption

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
4 / BATT 1 / B2B 44 / B2B 1 / SIMFLEX	VBATT, VB	5.75V	7.2V	–	Software limit
		4.8V	7.2V	8.7 +/–0.3V	Hardware limits (cut–off min, charging max)
		4.8V	7.2V	7.6 +/–0.3V	Hardware limits during a call

Table 3. Supply Voltages and Power Consumption (continued)

Pin / Conn.	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
14 / B2B 31 / B2B	VCHAR	10.0V	12.0	13.0V	Charger specifications, without load
	VA1	4.5V	4.65V	4.8V	Imax = 40mA
	VA2	4.5V	4.65V	4.8V	Imax = 80mA
	VA3	4.5V	4.65V	4.8V	Imax = 200mA
11 / B2B	VL1	4.7V	4.85V	5.0V	Imax = 150mA
	VL2	4.7V	4.85V	5.0V	Imax = 150mA
	VREF	4.55V	4.65V	4.75V	Imax = 5mA
16 / B2B	VF	11.4V	12V	12.6V	Flash programming voltage

Table 4. Digital control signals

6 / B2B	BACKLIGHT	0V		0.7V	Output low, backlights off	Display and keyboard illumination control
		4.7V	4.85V	5.0V	Output high, backlights on	
8 / B2B	RBUSRXD	3.6V	4.85V	5.0V	State ”1”	RBUS received data to CMT
		0V	0.2V	0.7V	State ”0”	
9 / B2B	RBUSTXD	3.6V	4.85V	5.0V	State ”1” 1 mA load	RBUS transmitted data from CMT
		0V	0.2V	0.7V	State ”0”	
12 / B2B	XPWRON	0V	0V	0.7V	Input low, power on/off	
			4.65V		Floating when inactive. A pull–up in PSL+.	
15 / B2B	BUZPWR	0V		0.7V	Input low, buzzer on	
		5.3V	7.2V	8.4V	Input high, buzzer off	
20 / B2B 19 / B2B 18 / B2B 17 / B2B	COL(3:0)	0V		0.7V	Output low	keyboard columns
		4.7V	4.85V	5.0V	Output high	

27 / B2B 26 / B2B 25 / B2B 24 / B2B	UIF(3:0)	0V		0.7V	Output/Input low	keyboard row lines/ display data lines
		4.7V	4.85V	5.0V	Output/Input high	
28 / B2B	UIF4	0V		0.7V	Output/Input low	keyboard row read/write strobe for LCD driver
		4.7V	4.85V	5.0V	Output/Input high	
29 / B2B	UIF5	0V		0.7V	Output/Input low	keyboard row LCD driver register select
		4.7V	4.85V	5.0V	Output/Input high	
30 / B2B	UIF6	0V		0.7V	Output/Input low	enable strobe for LCD driver
		4.7V	4.85V	5.0V	Output/Input high	
32 / B2B	DCLK	3.6V	4.85V	5.0V	State ”1”	DBUS clock 512 kHz
		0V	0.2V	0.7V	State ”0”	
33 / B2B	DSYNC	3.6V	4.85V	5.0V	State ”1”	DBUS sync 8 kHz
		0V	0.2V	0.7V	State ”0”	
34 / B2B	RDA	3.6V	4.85V	5.0V	State ”1”	DBUS received data to CMT
		0V	0.2V	0.7V	State ”0”	
35 / B2B	TDA	3.6V	4.85V	5.0V	State ”1” 1 mA load	DBUS transmitted data from CMT
		0V	0.2V	0.7V	State ”0”	
36 / B2B	M2BUS	0V		0.7V	Input low level	Isink<5m ABaud rate 9600 bits/s. (or double)
		3.0V		5.0V	Input high level	
		0V	0.2V	0.35V	Output low level	
		3.6V	4.85V	5.0V	Output high level	
38 / B2B	LID	3.3V		4.9V	Lid open	Cover switch status
		0.0V		1.0V	Lid closed	
2 / SIMFLEX	BUZZER	0V		0.7V	Output low, buzzer on	Buzzer on SIM flex
		5.3V	7.2V	8.4V	Output high, buzzer off	

6 / SIMFLEX	SIMCLK	3.6V	4.85V	5.0V	State ”1”	Clock for SIM card
		0V	0.2V	0.7V	State ”0”	
7 / SIMFLEX	SIMRESET	4.7V	4.85V	5.0V	Output high	Reset for SIM card
		0V		0.7V	Output low	
8 / SIMFLEX	VSIM	4.7V	4.85V	5.0V		SIM card reader supply voltage
9 / SIMFLEX	SIMDATA	0V		0.8V	Input low level	Data for SIM card
		2.0V		5.0V	Input high level	
		0V	0.2V	0.7V	Output low level	
		4.7V	4.85V	5.0V	Output high level	

Table 5. Battery monitoring signals

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maxi-mum	Unit / Notes
11 / SIMFLEX 12 / SIMFLEX	MICN MICP		5 mV_{rms}	19 mV_{rms}	Differential
3 / SIMFLEX 4 / SIMFLEX	EARN EARP		124 mV_{rms}	1.965 V_{rms}	Differential, $R_L = 32\Omega$
3 / B2B 4 / B2B	PHFMICN PHFMICP		5 mV_{rms}	19mV_{rms}	Differential
1 / PHF 2 / PHF	PHFEARP PHFEARN		1.0 V_{rms}	2.8 V_{rms}	Differential $R_L = 8\ \Omega$
41 / B2B	EXTMIC		200 mV_{rms}	530 mV_{rms}	minimum DC–level 2.0V.
42 / B2B	EXTEAR		160 mV_{rms}	410 mV_{rms}	minimum DC–level 2.0V.

AC Characteristics

Table 6. Audio Signals

Pin / Type	Line Symbol	Minimum	Typical / Nominal	Maximum	Unit / Notes
11 / SIM-FLEX 12 / SIM-FLEX	MICN MICP		5 mV_{rms}	19 mV_{rms}	Differential
3 / SIMFLEX 4 / SIMFLEX	EARN EARP		124 mV_{rms}	1.965 V_{rms}	Differential, R_L = 32Ω
3 / B2B 4 / B2B	PHFMICN PHFMICP		5 mV_{rms}	19mV_{rms}	Differential
1 / PHF 2 / PHF	PHFEARP PHFEARN		1.0 V_{rms}	2.8 V_{rms}	Differential R_L = 8 Ω
41 / B2B	EXTMIC		200 mV_{rms}	530 mV_{rms}	minimum DC–level 2.0V.
42 / B2B	EXTEAR		160 mV_{rms}	410 mV_{rms}	minimum DC–level 2.0V.

Table 7. Handportable audios, microphone

HPMIC 1kHz rms		NOTES
MRP pressure	+3 dBPa	5 cm from MIC
MIC pressure	–2 dBPa	about 5 dB attenuation
MIC output	5.0 mV	mic sensitivity –64 dB (6.3 mV/Pa) 0 dB = 1V/uBar 1uBar=0.1Pa
Codec gain	29 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–11 dBmO / 140 mVrms	0 dBmO = 490 mV

Table 8. Handportable earpiece

HPEAR 1 kHz rms		NOTES
Level	–6.0 dBmO / 980 mVrms	0 dBmO = 1965 mVrms
Codec gain	–18 dB nominal –8 dB max. volume	18 dB atten. Controllable 0...–30 dB. Maximum volume +10 dB
Codec output	120 mVrms nominal 390 mVrms max.volume	
Earpiece pressure	+6 dBPa nominal +16 dBPa max. volume	Earpiece impedance 32Ω + 20Ω series resistance in CMT.

Table 9. Personal HF microphone

PHFMIC 1kHz rms		NOTES
MRP pressure	+14 dBPa	50 cm from MIC
MIC pressure	–6 dBPa	about 20 dB attenuation
MIC output	3.1 mVrms	mic sensitivity –64 dB (6.3 mV/Pa) 0 dB = 1V/uBar 1uBar=0.1Pa
Codec gain	30.5 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–13.5 dBmO / 105 mVrms	0 dBmO = 490 mVrms

Table 10. Personal HF speaker

PHFEAR 1 kHz rms		NOTES
Level	–6.0 dBm0 / 980 mVrms	0 dBm0 = 1965 mVrms
Codec gain	–14 dB nominal –6 dB max. volume	14 dB attenuation. Controllable 0...–30 dB. Maximum volume +8 dB
Output attenuation	6 dB	6 dB attenuation because of single ended output.
Codec output	100 mVrms nominal 245 mVrms maximum	
Booster gain	18 dB	
Speaker input	0.78 Vrms nominal 1.95 Vrms maximum	80 mW average / 8Ω / Bridge tied load. 480 mW average / 8Ω / Bridge tied load.
Pressure	–19 dBPa nominal –11 dBPa maximum	50 cm from speaker. Speaker sensitivity 80 dB/W/1m (Foster T028S21). 0dB = –94 dBPa (20 μPa)

Table 11. Accessory HS microphone

HSMIC 1kHz rms		NOTES
MRP pressure	+3 dBPa	5 cm from MIC
MIC pressure	–2 dBPa	about 5 dB attenuation
MIC output	6.3 mVrms	mic sensitivity –62 dB (7.9 mV/Pa) 0 dB = 1V/uBar 1uBar=0.1Pa
Handset gain	27 dB	Flat mic response
Accessory level	140 mVrms	
HFJ gain	0 dB	
Cable level	140 mVrms	
Attenuation on system board	21 dB	

Table 11. Accessory HS microphone (continued)

HSMIC 1kHz rms		NOTES
Codec input level	12.5 mVrms	
Codec gain	26 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–6 dBm0 / 250 mVrms	0 dBm0 = 490 mVrms

Table 12. Accessory HS earpiece

HSEAR 1 kHz rms		NOTES
Level	–6.0 dBm0 / 980 mVrms	0 dBm0 = 1965 mVrms
Codec gain	–6 dB	With maximum gain
Output attenuation	6 dB	6 dB attenuation because of single ended output.
Cable level	245 mVrms	min. impedance 1 kΩ
HFJ gain	0 dB	
Accessory level	245 mVrms	
Handset gain	1 dB minimum 18 dB maximum	Hanset gain (–5...+12) dB + 6 dB from single–side to differential conversion
EAR amp. output	310 mVrms minimum 1.95 Vrms maximum	Measured differentially
Earpiece pressure	+1 dBPa minimum +18 dBPa maximum	

Table 13. Accessory HF microphone

HFMIC 1 kHz rms		NOTES
MRP	+15 dBPa	50 cm from MIC
MIC	–5 dBPa	about 20 dB atten.
MIC output when HFJ connected	2.0 mVrms	MIC sensitivity –65 dB (5.6 mV/Pa) (mic output level 3.3 mV without load)
HFJ gain	40 dB	
Cable level	200 mVrms	
Attenuation on system board	21 dB	
Codec input level	18 mVrms	
Codec gain	23 dB	Fixed 20 dB + programmable 0...22.5 dB
Level	–6 dBm0 / 250 mVrms	0 dBm0 = 490 mVrms

Table 14. Accessory HF speaker

HFEAR 1 kHz rms		NOTES
Level	–10 dBm0 / 620 mVrms	0 dBm0 = 1965 mVrms
Codec gain	–16 dB nominal	
Output attenuation	6 dB	6 dB attenuation because of single ended output.
Cable level	50 mVrms nominal	minimum impedance 1kΩ
HFJ gain	27 dB	
HFJ output level	1.1 Vrms nominal	
Pressure	about –2 dBPa	50 cm from loudspeaker

Connectors

Connectors to other modules of the product

Table 15. PDA board to board connector (B2B)

Signal Name	Pin(s)	Notes
VB	1,44	Battery voltage to the PDA module.
GND	2,5,7,10,13,21, 22,23,37,39,40	Ground
PHFMICN	3	PHF microphone (negative node)
PHFMICP	4	PHF microphone (positive node)
BACKLIGHT	6	Backlights on/off
RBUSRXD	8	RBUS receive data
RBUSTXD	9	RBUS transmit data
VL1	11	Logic supply voltage (4.7–5.0V)
XPWRON	12	Power key (active low)
VCHAR	14,31	Battery charging voltage.
BUZPWR	15	PWM signal buzzer control input from PDA module
VF	16	Programming voltage for flash.
COL(3:0)	20,19,18,17	Lines for keyboard write
UIF(3:0)	27,26,25,24	Lines for keyboard read and LCD–controller data
UIF4	28	Line for keyboard read and LCD–controller read/write strobe
UIF5	29	Line for keyboard read and LCD–controller data/instruction register selection
UIF6	30	LCD–controller enable strobe
DCLK	32	DBUS–data clock
DSYNC	33	DBUS–data bit sync clock

Table 15. PDA board to board connector (B2B) (continued)

Signal Name	Pin(s)	Notes
RDA	34	DBUS received data from the accessories
TDA	35	Transmitted DBUS–data to the accessories
M2BUS	36	Serial bidirectional data and control between the CMT and accessories.
LID	38	Cover switch state from PDA to CMT
EXTMIC	41	External audio input from accessories or handsfree microphone. Multiplexed with junction box connection indication. 16.8k pull down in CMT
EXTEAR	42	External audio output to accessories or handsfree speaker. 100kΩ pull–down in CMT to turn on the junction box.
AGND	43	Analog ground for accessories. Connected directly to digital ground on the PCB.

Table 16. PHF speaker connector

Signal Name	Pin(s)	Notes
PHFEARN	1	PHF speaker, negative node
PHFEARP	2	PHF speaker, positive node

Table 17. SIMFLEX Connector

Signal Name	Pin	Notes
VBATT	1	Battery voltage for buzzer
BUZZER	2	Excitation for buzzer (pull–down)
EARN	3	Differential audio for the earpiece
EARP	4	
GND	5,10	Ground
SIMCLK	6	Clock for SIM data
SIMRESET	7	Reset for SIM
VSIM	8	SIM voltage supply
SIMDATA	9	Serial data for SIM
MICN	11	Differential audio from the microphone
MICP	12	

Connectors out of Transceiver Unit

Table 18. Battery connector

Signal Name	Pin	Notes
BGND	1	Battery ground
TBAT	2	Battery temperature
BTYPE	3	Battery type
VB	4	Battery voltage

Internal Signals and Connections

Table 19. Signals Between RF and D2CA ASIC (MCM2)

Signal Name	Function	Notes
SCLK	Synthesizer clock	From ASIC to RF
SDATA	Synthesizer data	From ASIC to RF
SENA1	UHF and VHF PLL enable	From ASIC to RF
RXPWR	RX supply voltage ON/OFF	From ASIC to RF
SYNTHPWR	Supply voltage ON/OFF	From ASIC to RF
TXPWR	TX supply voltage ON/OFF	From ASIC to RF
TXP	Transmitter power control enable	From ASIC to RF
RFC	26 MHz clock from RF to baseband	From RF to ASIC

Table 20. Signals Between RF and RFI (MCM2)

Signal Name	Function	Notes
AFC	Automatic frequency control voltage	From RFI to RF
TXC	TX transmit power control voltage and RX automatic gain control voltage	From RFI to RF
TXQP,TXQN	differential TX quadrature signal	From RFI to RF
TXIP,TXIN	differential TX in–phase signal	From RFI to RF
PDATA0	LNA gain control	From RFI to RF
RXQ	RX quadrature signal (13 MHz)	From RF to RFI
RXI	RX inphase signal (13 MHz)	From RF to RFI
RFIREF	4.096 V reference voltage	From RFI to RF

Table 21. Signals Between RF and CTRLU (MCM1)

Signal Name	Function	Notes
TRF	RF temperature sensor	From RF to CTRLU

Table 22. Signals Between RF and PWRU

Signal Name	Function	Notes
VREF	Supply voltage for VCXO	From PWRU to RF
VBATT	Battery voltage	From PWRU to RF
GND	Ground	Common ground

Circuit Descriptions

Power Distribution

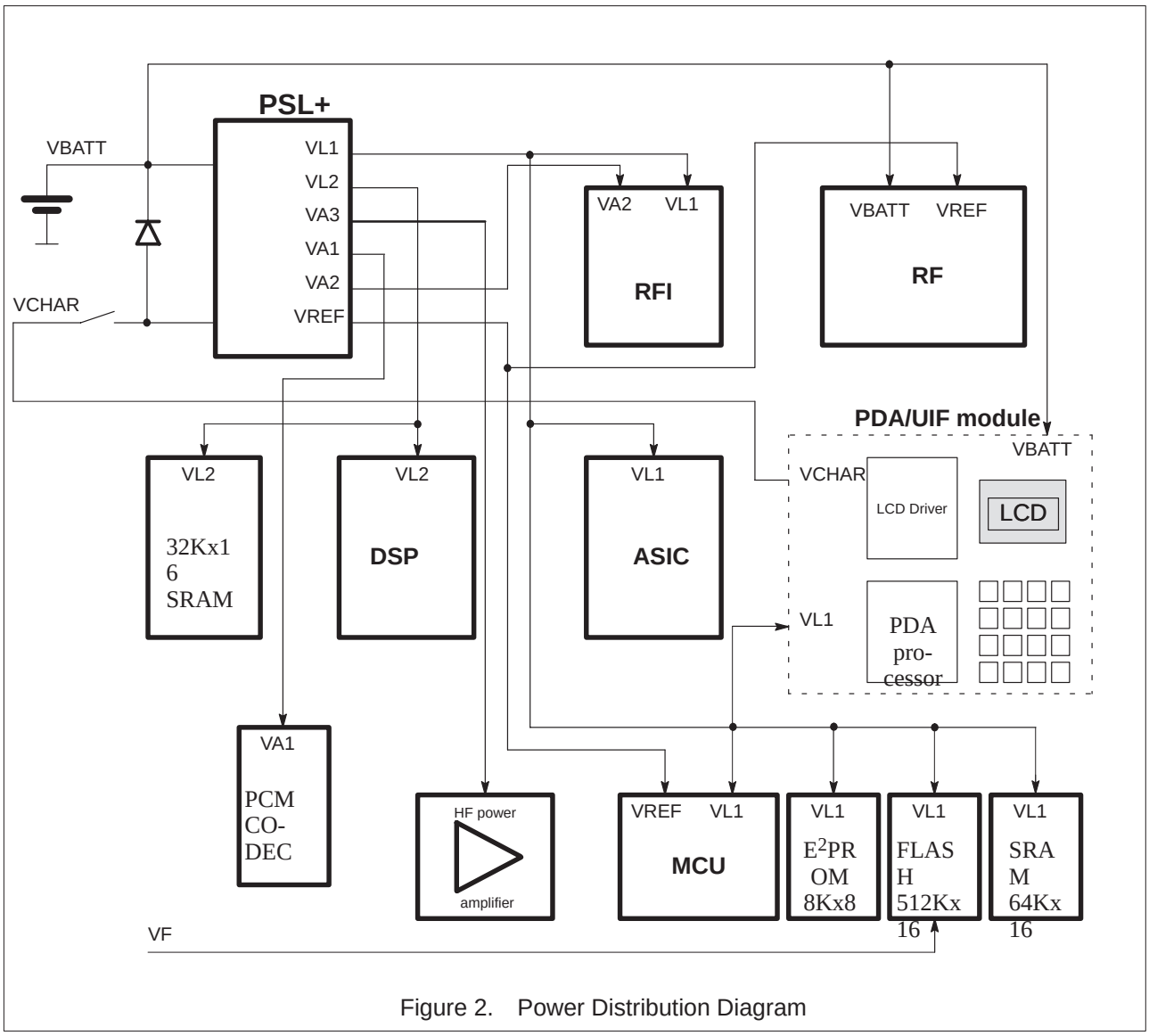

Figure 2. Power Distribution Diagram

Clocking scheme

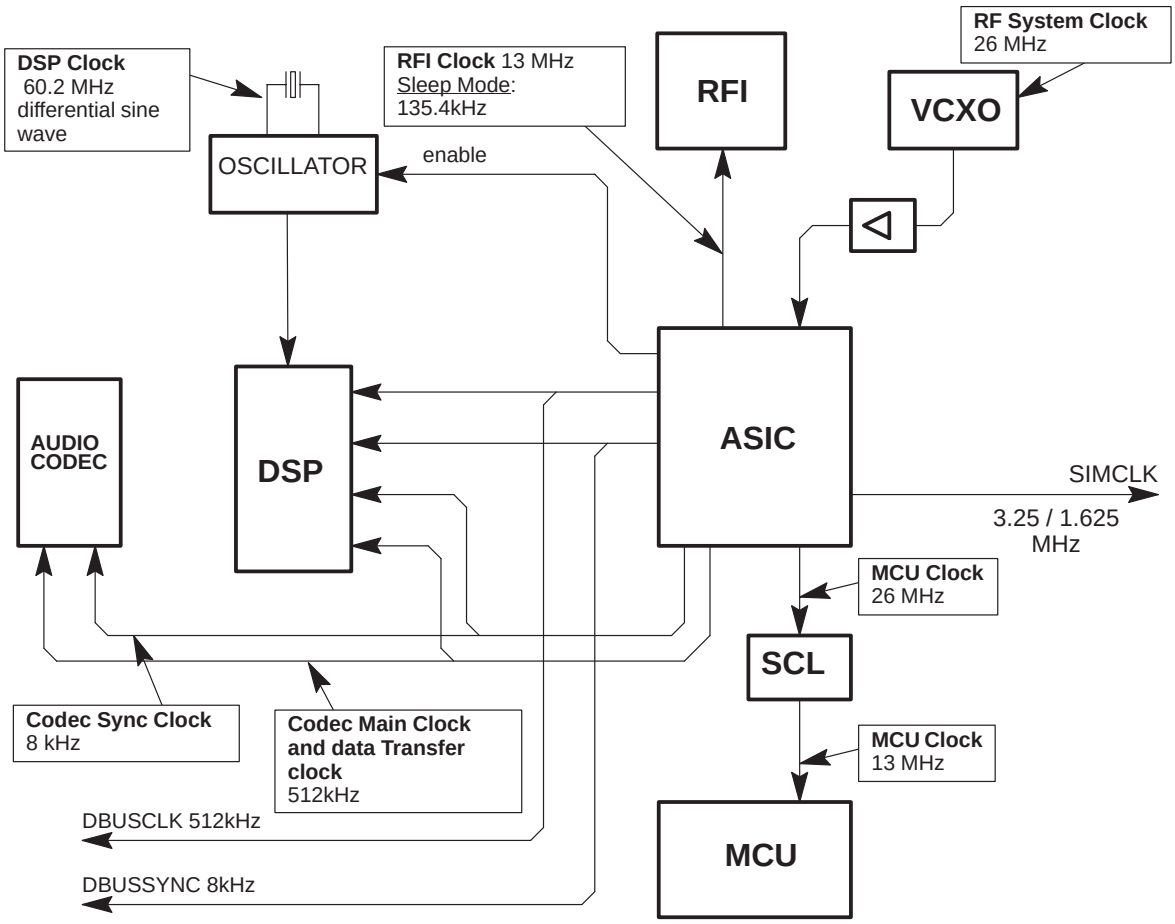

Figure 3. Clocking Scheme

Most of the clocks are generated from the 26 MHz VCXO frequency by the ASIC:

– *26 MHz clock for the MCU*. SCL divides this by two and supplies a 13 MHz clock to the MCU.
– *13 MHz for the RFI.* The ASIC also generates 135.4 kHz sleep mode clock for the RFI.
– *3.25 MHz clock for SIM*. When there is no data transfer between the SIM card and the baseband the clock can be reduced to 1.625 MHz. Some SIM cards also allows the clock to be stopped in that mode.
– *512 kHz main clock for the codec* and for the data transfer between the DSP and the codec.
– *8 kHz synchronisation clock for data transfer* between the DSP and the codec.
– *512 kHz clock and 8 kHz sync. clock for the DBUS data transfer*

The DSP has its own crystal oscillator which can be turned off and on by the ASIC. The DSP uses differential sinusoidal clock. The frequency is 60.2 MHz.

The MCU generates 8 kHz clock to the codec for the control data transfer.

In the idle mode all the clocks can be stopped except 26 MHz main clock coming from the VCXO.

Reset and power control

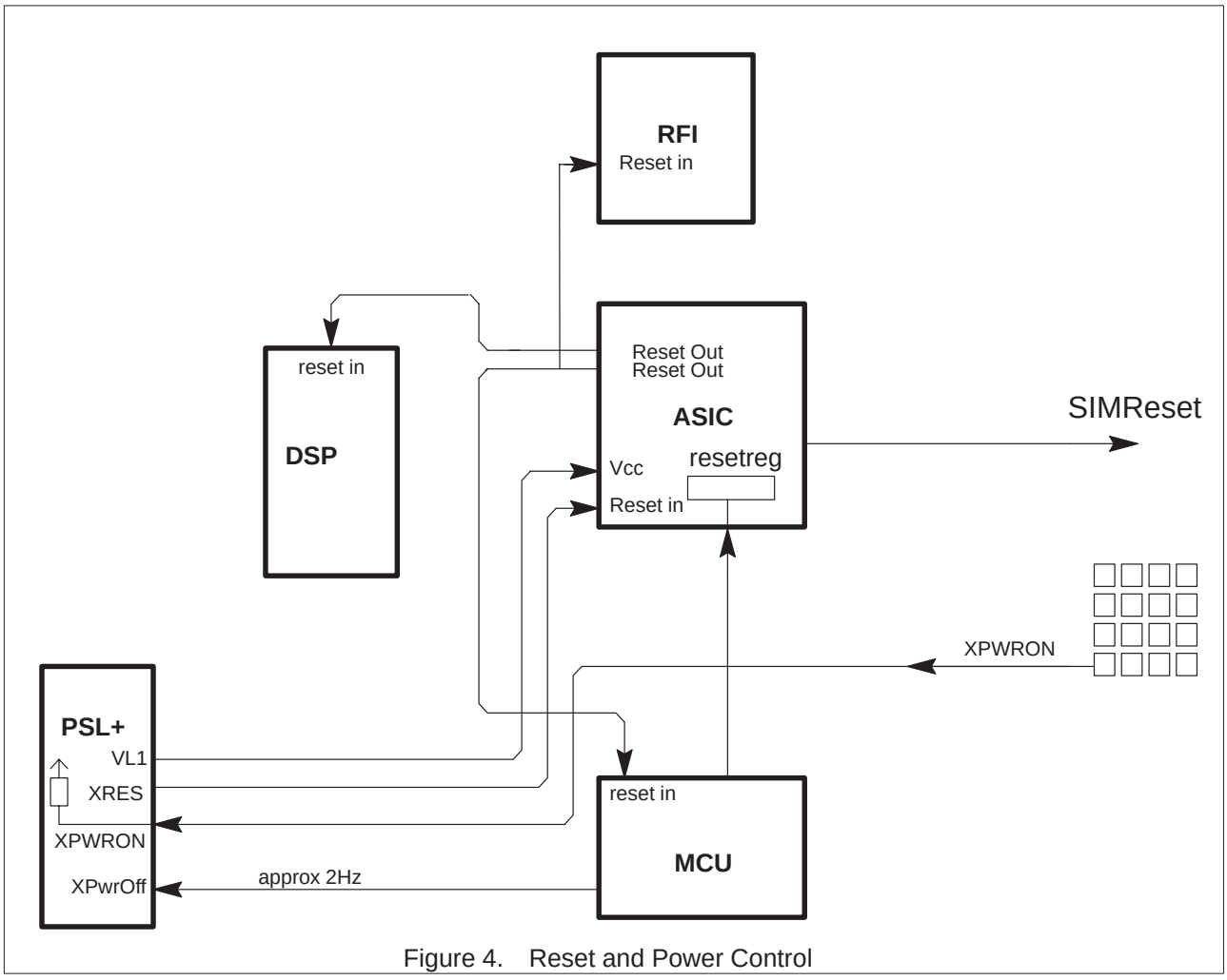

Figure 4. Reset and Power Control

There are three different ways to switch power on:

Pulling the XPWRON line down e.g by pressing the power key. The PSL+ detects that and switches the power on.

Charger detection on PSL+ detects that charger is connected and switches power on

PSL+ will switch power on when the battery is connected. After that the MCU will detect if power key is pressed or charger connected. If not the power will be switched off

All devices are powered up at the same time by the PSL+. It supplies the reset to the ASIC at power up. The ASIC starts the clocks to the DSP and the MCU. After about 100 ms the PSL+ releases the reset to ASIC.

ASIC releases the resets to MCU and RFI after 256 13 MHz clock cycles. DSP reset release time from DSP clock activation can be selected from 0 to 255 13MHz clock cycles. In our case it is 255. SIM reset release time is according to GSM SIM specifications.

To turn off power for the phone, the user presses the PWR key. The MCU detects this. The MCU cuts off any ongoing call, exits all tasks, acts inoperative to the user and leaves the PSL+ watchdog without resets. After power–down delay, the PSL+ cuts off the supply from all circuitry.

In the acting dead state the phone looks to the user like it is off (lights are off and the display is blank) but internally the baseband is powered and communication via RBUS is possible. The RF is not powered in acting dead state.

If charger is connected in the off state, the phone enters the acting dead state, but the charging indicator in the UI module shows to the user that the phone is being charged.

Watchdog system

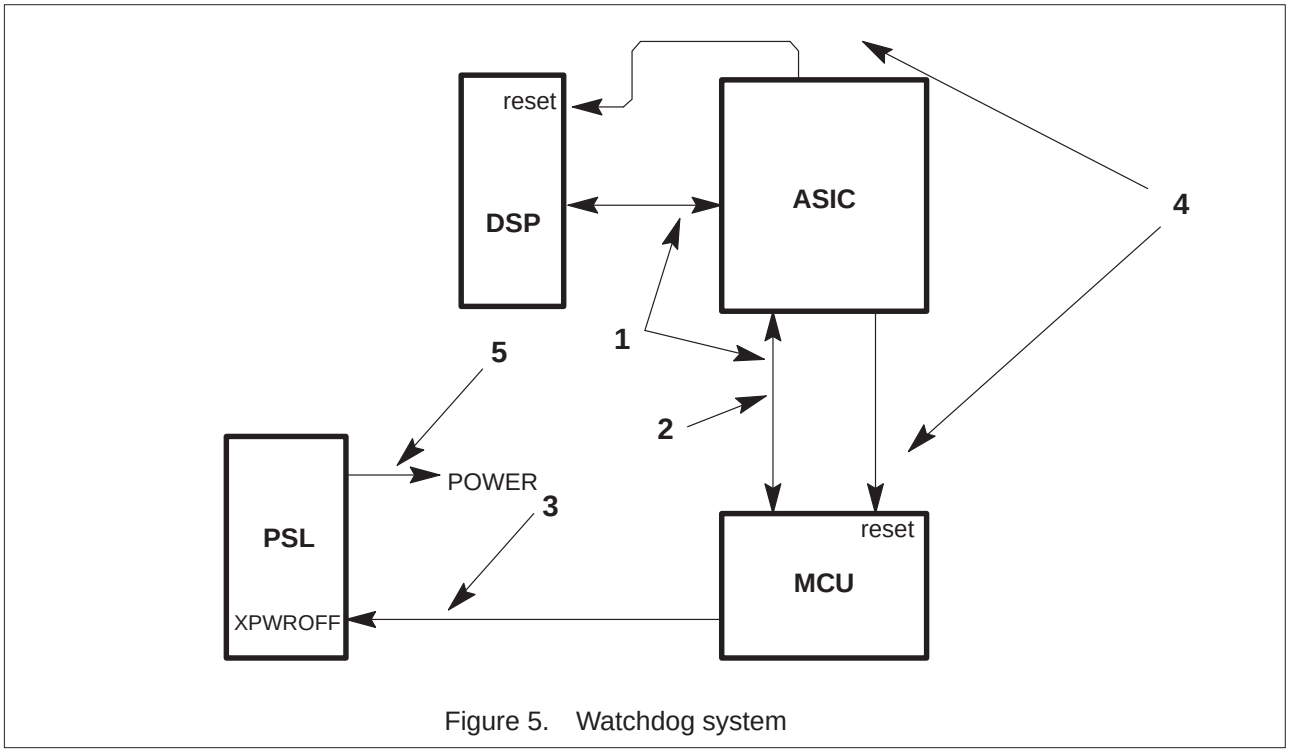

Figure 5. Watchdog system

Normal operation:

1. MCU tests DSP
2. MCU updates ASIC watchdog timer (> 2Hz)
3. MCU pulses the XPWROFF input on the PSL+ (about 2Hz)

Failed operation:

4. ASIC resets MCU and DSP after about 0.5 s failure
5. PSL+ switches power off about 5 s after the previous XPWROFF pulse

CTRLU

Introduction

The Control block contains a microcomputer unit (MCU) and five memory circuits (2xFLASH, 2xSRAM and EEPROM), a 20–bit address bus and a 16–bit data bus. Physically the CTRLU resides entirely on MCM1.

Main Features of the CTRLU Block

MCU functions:

– system control
– communication control
– user interface functions
– GSM data encoding and decoding
– authentication
– RF monitoring
– power up/down control
– accessory monitoring
– battery monitoring and charging control
– self–test and production testing
– flash loading

Technical specifications

Table 23. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL1	Power supply voltage for CTRLU block	PWRU
VREF	Reference voltage for MCU AD–converter	PWRU
VFF	Programming voltage for flash memory	B2B Conn
VBATDET	Battery voltage detection	PWRU
VC	Charger voltage monitoring	PWRU
RESETX	Reset signal for MCU	ASIC
NMI	Non–maskable interrupt request	ASIC
MCUCLK	Main clock for MCU	ASIC
IRQX	Interrupt request	ASIC
PCMCDO	Audio codec control data receiving	AUDIO
TRF	RF–module temperature detection	RF
LID	Cover open/closed detection (HOOK A/D input).	B2B Conn
RBUSRXD	RBUS receive data	B2B Conn
TBAT	Battery temperature monitoring	Battery Conn

Table 23. External Signals and Connections, Inputs (continued)

Signal Name	Signal description	From
BTYPE	Battery size identification	Battery Conn
JCONN	Junction box connection identification	AUDIO
MBUSIN	MBUS RX data	B2B Conn

Table 24. External Signals and Connections, Outputs

Signal Name	Signal description	To
XPWROFF	Power off control, PSL+ watchdog reset	PWRU
PWM	Charger switch on/off control	PWRU
WSTROBEX	MCU write strobe	ASIC
RSTROBEX	MCU read strobe	ASIC
MCUAD(19:16) MCUAD(4:0)	Parts of MCU address bus	ASIC
MRBUSDET	MBUS and RBUS activity detection	ASIC
PCMCLK	Clock for audio codec control data transfer	AUDIO
PCMCDI	Audio codec control data transmitting	AUDIO
XSELPCMC	Chip select for audio codec	AUDIO
RBUSTXD	RBUS transmit	B2B Conn
BACKLIGHT	LCD and display backlight on/off control	B2B Conn
AMP_PWR	PHF amplifier ON/STDBY	AUDIO
VOLTLIM	Charging voltage limitation during call	PWRU
MBUSOUT	MBUS TX data (open drain)	B2B Conn

Table 25. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
MCUDA(15:8)	MCU’s 8–bit data bus	ASIC

Block description

– MCU Memories

The MCU has a 20 bits wide address bus A(19:0) and an 16–bit data bus with memories. The address bits A(19:13) are used for chip select decoding. The decoding is done inside the SCL in CTRLU submodule. Hitachi HD6475388 processor has internal ROM and RAM memories.

Memory Map

Table 26. Memory Map

PAGE	ADDRESS	FPAGE[1:0]= 00	FPAGE[1:0]=01	FPAGE[1:0]=10
0	00000 0EE7F	INTERNAL ROM 60 Kbytes (16 bit)		
	0EE80 0F67F	EXTERNAL ADDRESS SPACE		
	0F680 0FE7F	INTERNAL RAM 2 Kbyte (16 bit)		
	0FE80 0FFFF	REGISTER FIELD 384 bytes		
1	10000 1FFFF	RAM 64 Kbytes (16 bit)		
2 – 11	20000 BFFFF	FLASH 640 Kbytes (16 bit) FA[19:17]=001...101		
12 – 13	C0000 DFFFF	FLASH 128 Kbytes (16 bit) FLASH page 0 FA[19:17]=110	FLASH 128 Kbytes (16 bit) FLASH page 1 FA[19:17]=111	FLASH 128 Kbytes (16 bit) FLASH page 2 FA[19:17]=000
14	E0000 EDFFF	SRAM 56 Kbytes (16 bit)		
	EE000 EFFFF	EEPROM 8 Kbytes (8 bit)		
15	F0000 F001A FFFFF	ASIC 26 bytes (8 bit)		

Table 27. Chip Select Generation

A19	A18	A17	A16	A15	A14	A13	CHIP SELECT	NOTES
0	0	0	1	X	X	X	SRAM (page 1)	32K x 16 bit area
1	1	1	0	0	X	X	SRAM (page 14)	28K x 16 bit area
1	1	1	0	X	0	X	SRAM (page 14)	
1	1	1	0	X	X	0	SRAM (page 14)	
1	1	1	0	1	1	1	EEPROM (page 14)	8K x 8 bit area
1	1	1	1	X	X	X	ASIC (page 15)	64K x 8 bit area
0	0	1	X	X	X	X	FLASH (pages 2 – 3)	320K x 16 bit area
0	1	X	X	X	X	X	FLASH (pages 4 – 7)	
1	0	X	X	X	X	X	FLASH (pages 8 – 11)	
1	1	0	X	X	X	X	FLASH (pages 12 – 13)	64K x 16 bit area, paged with FPAGE[1:0]

Table 28. FLASH address generation on pages 12 – 13

Address and page select inputs					FLASH address (highest bits)			NOTES
A19	A18	A17	FPAGE1	FPAGE0	FA19	FA18	FA18	
1	1	0	0	0	1	1	0	FLASH page 0
1	1	0	0	1	1	1	1	FLASH page 1
1	1	0	1	0	0	0	0	FLASH page 2
1	1	0	1	1	0	0	1	Reset SCL clk divider. **NEVER USE THIS !**

– Flash programming

In flash programming a special flash programming box and a PC is needed. Loading is done through a test connector of PDA module using the same serial channel as RBUS. PDA module should not use RBUS during flash loading. First MCU goes to minimum mode (MBUS command from PC or if MBUS is connected to EXTMIC/JCONN line in power up). Then the flash software is loaded from PC to flash loading box. After the loading is complete the flash loading from box to CMT can be started by MBUS command from PC to the MCU. After that the MCU asks the test box to start flash loading to baseband. The box supplies 12 V programming voltage for flash and starts to send 250 bytes data blocks to the MCU via RBUSRxD line. The baud rate is 406 kbit/s. The MCU calculates the check sum, sends acknowledge via RBUSTxD line and sends the data to flash. When all the data is loaded the CMT makes reset and tells the flash loading box if the loading was succeeded or not. Only PSL+, ASIC, SCL and MCU must be active during the loading.

– CTRLU – PWRU

MCU controls the watchdog timer in PSL+. It sends a positive pulse at approximately 2 Hz to XPWROFF pin of the PSL+ to keep the power on. If MCU fails to deliver this pulse, the PSL+ will remove power from the system. MCU also controls the charger on/off switching in the PWRU block. When power off is requested or MCU leaves PSL+ watchdog without reset. after the watchdog time has elapsed the PSL+ cuts off the supply voltages from the phone.

– CTRLU – ASIC

MCU and ASIC have a common 8–bit data bus and a 9–bit address bus. Bits A(4:0) are used for normal addressing. ASIC controls the main clock, main reset and interrupts to MCU. The 26 MHz MCUCLK is divided by two in SCL and the resulting 13 MHz clock is supplied to the MCU. RESETX resets everything in MCU except the contents of the RAM. IRQX is a general purpose interrupt request line from ASIC. After IRQX request the interrupt register of the ASIC is read to find out the reason for interrupt. NMI is used only to wake up MCU from software standby mode.

– CTRLU – DSPU

MCU and DSP communicate through ASIC. ASIC has an MCU mailbox and a DSP mailbox. MCU writes data to DSP mailbox where DSP can only read the incoming data. In MCU mailbox the data transfer direction is the opposite. When power is switched on the MCU loads data from the flash memory to DSP‘s external memory through this mailbox.

– CTRLU – AUDIO

When the the chip select signal XSELPCMC goes low, MCU writes or reads control data to or from the speech codec registers at the rate defined by PCMCLK. PCMCDI is an output data line from MCU to codec and PCMCDO is an input data line from codec to MCU. The AMP_PWR signal is used for switching the Personal Hands–Free amplifier between On and Standby modes.

– CTRLU – RF/BATTERY Monitoring

MCU has internal 12 channel 10 bit AD converter. Following signals are used for monitoring battery, charging and RF:

BTYPE	battery size
TBAT	battery temperature
VBATDET	battery voltage
VC	charging voltage
TRF	RF temperature

– CTRLU – Keyboard and LCD Driver Interface

MCU and User Interface communication is controlled through ASIC.

– CTRLU – ACCESSORIES

MBUS is used to control external accessories. This interface can also be used for factory testing and maintenance purposes.

There are also some control and indication signals for the accessories:

JCONN is used to indicate that junction box is connected. JCONN is actually the DC–level of the EXTMIC signal. Phone can also enter minimum mode when MBUS is connected to EXTMIC line.

Main components

– Hitachi H8/538

H8/538 is a CMOS microcontroller unit (MCU) which includes a static CPU core and on–chip supporting modules with 16–bit architecture. The data bus to outside world is 16 bits wide.

– SCL ASIC
  – MCU address decoding and memory chip select generation
  – FLASH and system ASIC address mapping
  – MBUS interface
  – MBUS/RBUS activity detection
  – MCU clock division from 26 MHz to 13 MHz
– 512k*16bit FLASH memory
  – two 512Kx8 FLASH chips
  – 65 ns maximum read access time
  – contains the main program code for the MCU; part of the DSP program code also located on FLASH
– 64k*16bit SRAM memory
  – two 64Kx8 SRAM chips
  – 65 ns maximum read access time
– 8k*8bit EEPROM memory
  – 150 ns maximum read access time
  – contains user defined information

PWRU

Introduction

The power block creates the supply voltages for the baseband block and contains the charging switch and its control electronics.

Technical description

Table 29. External Signals and Connections, Inputs

Signal Name	Signal description	From
XPWRON	Power on switch	B2B Conn
XPWROFF	PSL+ watchdog updating; power off control	CTRLU
VBATT	Battery voltage	Battery conn

Table 29. External Signals and Connections, Inputs (continued)

Signal Name	Signal description	From
PWM	Charger on/off control	CTRLU
VCHAR	Charging voltage	B2B conn
VOLTLIM	Charging voltage limitation during call; affects HW voltage limit	CTRLU

Table 30. External Signals and Connections, Outputs

Signal Name	Signal description	To
XRES	Master reset	ASIC
VL1	Logic supply voltage. Max 150 mA.	CTRLU, ASIC, RFI, UIF
VL2	Logic supply voltage. Max 150 mA.	DSPU
VA1	Analog supply voltage for AUDIO block. Max 40 mA.	AUDIO
VA2	Analog supply voltage for RFI. Max 80 mA.	RFI
VA3	Analog supply voltage for PHF power amplifier. Max 200 mA.	AUDIO
VREF	Reference voltage 4.65V ∓2%. Max. 5mA.	CTRLU,RF
VBATDET	Switched VBATT divided by 2	CTRLU
CHRDET	Charger detect output	ASIC
VCHARO	Charging voltage to battery	Batt conn
VC	Attenuated VCHAR	CTRLU

Block description

The PSL+ IC produces the following supply voltages:

VL1	150 mA for logic
VL2	150 mA for logic
VA1	40 mA for audios
VA2	80 mA for RFI
VA3	200 mA for PHF booster
VREF	5mA reference

In addition, it has internal watchdog, voltage detection and charger detection functions. The watchdog will cut off output voltages if it is not reset once in every 5 (+/–1?) seconds. The voltage detector resets the phone if the battery voltage falls below 4.8 V (+/–0.2V). The charger detection starts the phone if it is in power–off state when the charging voltage is applied.

The charging electronics is controlled by the MCU. When the charging voltage is applied to the phone and the phone is powered up, the MCU detects it and starts controlling charging. If MCU detects too high charging voltage (over 10 volts) or current (over 78 A/D bit difference between VC and VBATDET) it will cut off the charging. The phone will accept charging voltages from 5 to 13 volts.

If the phone is in power–off state, the PSL+ will detect the charging voltage and turn on the phone. If the battery voltage is high enough the reset will be released and the MCU will start controlling charging. If the battery voltage is too low the phone stays in reset state and the charging control circuitry will pass small charging current to the battery. When the battery voltage has reached 5.5 V (+/– 0.2 V) the reset will be removed and the MCU starts controlling charging.

MCU controls the charging with pulse width modulation output. Charging voltage is limited by hardware in normal operation to 8.9 V and during a call to 7.6 V.

Battery and charging voltages are calibrated in production; 6V is fed to the battery and charger pin and the MCU‘s A/D converter values are stored to EEPROM.

Main components

– PSL+ ASIC (N230)

  Generates voltages, contains power on switch, charger and battery voltage detector and watchdog.

– transistors BCP69–25 (V250), BCV27 (V253,V254), BCW30 (V255) and Schottky STPS340U (V251)

  These components are used for implementing the charging switch.

– transistors BCX51 (V231) and BCP69–25 (V230, V232)

  External output transistors for VL1/VL2 and VA3 regulators in PSL+.

DSPU

Introduction

The DSPU performs of the low–level digital signal processing and control tasks required in channel monitoring and speech and data calls. The DSPU resides physically both in MCM2 (DSP and RAMs) and on CMT motherboard (clock generator and Schottky diode AND gate). Main interfaces of the DSPU:

– MCU via ASIC mailbox

– ASIC

– audio codec

– data bus interface (DBUS) for tracing purposes

– digital audio interface (DAI) for type approval measurements

Main features of the DSP block:

- speech processing
  - speech coding/decoding
    - RPE–LTP–LPC (regular pulse excitation long term prediction linear predictive coding)
  - voice activity detection (VAD) for discontinuous transmission (DTX)
  - comfort noise generation during silence
  - acoustic echo cancellation
- channel coding and transmission
  - block coding (with ASIC)
  - convolutional coding
  - interleaving
  - ciphering (with ASIC)
  - burst building and writing it to ASIC
- Reception
  - reading A/D conversion results from ASIC
  - impulse response calculation
  - matched filtering
  - bit detection (with Viterbi on ASIC)
  - deinterleaving of soft decisions
  - convolutional decoding (with Viterbi)
  - block decoding (with ASIC)
- Adjacent cell monitoring
  - signal strength measurements
  - neighbour timing measurements
  - neighbour parameter reception
- control functions
  - RF controls
    - synthesizer control
    - power ramp programming
    - automatic gain control (AGC)
    - automatic frequency control (AFC)

- frame structure control
  - control of operations during a TDMA frame (with ASIC)
  - control of multiframe structure
  - channel configuration control
- data functions
  - RLP CRC calculation
  - fax V110 frame encode/decode
- test functions
  - functions for RF measurements
  - debugging functions for product development

Technical description

Table 31. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL2	Logic supply voltage. Max 150 mA.	PWRU
DSPCLKEN	Clock enable for DSP clock oscillator circuit	ASIC
DSP1RSTX	Reset for the DSP	ASIC
PCMDATRCLKX	PCM data input clock DBUS data input clock	ASIC
PCMCOSYCLKX	PCM data bit sync clock	ASIC
CODEC_CLK	PCM data output clock	ASIC
PCMOUT	Received audio in PCM format	AUDIO
DBUSCLK	DBUS data output clock	ASIC
DBUSSYNC	DBUS data bit sync clock	ASIC
RDA	DBUS received data	B2B Conn.
INT0, INT1	Interrupts for the DSP	ASIC

Table 32. External Signals and Connections, Outputs

Signal Name	Signal description	To
PCMIN	Transmitted audio in PCM format	AUDIO
IOX	I/O enable. Indicates access to DSP I/O address space.	ASIC
RWX	Read/Write control	ASIC
DSPAD(16:0)	Address bus and control signals	ASIC
TDA	DBUS transmit data	B2B Conn.

Table 33. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
DSPDA(15:0)	16–bit data bus	ASIC

Block description

The DSPU communicates with the CTRLU through a mailbox in the D2CA ASIC. The software for the external memories are loaded through this mailbox in start up.

The DSP includes two serial buses. One is used for digitized speech transfer between the DSP and the codec. The other is used as an external data bus and it is connected to the B2B connector. This bus can be used for DSP tracing in product development and also as a digital audio interface (DAI) in audio type approval measurements. The clocks (512 kHz main clock and 8 kHz sync. clock) are generated by the D2CA ASIC.

In transmit mode the DSP codes the speech and routes the resulting transmit slots to the D2CA. The D2CA ASIC controls timing, and at specified intervals sends these bits to the RFI for D/A conversion.

In digital receive mode the RFI A/D converts the IF signal from the RF unit under the control of the D2CA. The DSP controls the D2CA and receives the converted samples. The received bits are detected from these samples in DSPU with the aid of some HW accelerators in ASIC. After channel and speech decoding, the bits are converted into an analog signal in the PCM codec. The echo cancellation algorithms of the handportable and Hands–Free modes are also performed in DSPU when needed.

In the case of the data or fax call the DSP performs CRC calculation or FAX V110 frame encoding/decoding instead of the speech encoding/decoding. Channel encoding/decoding and demodulation are performed in DSPU in this case also.

The DSP controls the RF through the D2CA ASIC, where all necessary timing functions are implemented, and control I/O lines are provided eg. for synthesizer loading.

The DSP emulator can be connected to DSP pins TCK, TMS, TDO, TDI, GND and VDD (JTAG standard).

Main components

- AT&T DSP1616–X11
    - Digital signal processor with 12kword internal ROM. The DSP locates physically in MCM2.
- Two 32k *8 70ns SRAMs for DSP external memory. The SRAM’s locate physically in MCM2.
- 60.2 MHz crystal oscillator to generate differential small signal clock for the DSP

AUDIO

Introduction

The AUDIO block contains an audio codec and a booster amplifier together with some peripheral components. The codec contains microphone and earpiece amplifiers and all the necessary switches for routing. The codec is controlled by the MCU. The PCM data comes from and goes to the DSP. The booster amplifier for the Personal Hands–Free (PHF) is connected to one of the codec's outputs. Physically the codec resides in MCM2 while the other parts are assembled on the CMT motherboard.

Technical specification

Table 34. External Signals and Connections, Inputs

Signal Name	Signal description	From
VA1	Analog supply voltage. Max 40 mA.	PWRU
VA3	Analog supply voltage for the PHF power amplifier. Max 200 mA.	PWRU
PCMIN	Received audio in PCM format	DSPU
SYNC	8kHz codec frame sync	ASIC
CODEC_CLK	512kHz codec main clock	ASIC
PCMCDI	Audio codec control data	CTRLU
PCMCLK	Clock for audio codec control data transfer	CTRLU
XSELPCMC	Audio codec chip select	CTRLU
AMP_PWR	PHF power amplifier control	CTRLU
MICN, MICP	Differential handportable microphone signal	SIM Conn
EXTMIC	External microphone signal	B2B Conn
PHFMICN, PHFMICP	Differential Personal Hands–Free microphone signal	B2B Conn

Table 35. External Signals and Connections, Outputs

Signal Name	Signal description	To
PCMOUT	Transmitted audio in PCM–format	DSPU
PCMCDO	Audio codec control data	CTRLU
JCONN	Junction box connected signal (multiplexed with EXTMIC)	CTRLU
EARN, EARP	Received audio to the earphone, differential signal	SIMFLEX Conn
EXTEAR	Received audio to the external accessories	B2B Conn
PHFEARN, PHFEARP	Received audio to the Personal Hands–Free speaker, differential signal	PHF Conn

Block description

The codec has three microphone inputs and two earphone outputs. The microphone inputs from handportable and PHF microphones plus the external audio input can be therefore connected directly to the codec. The handportable earphone output and external audio are also connected directly to the codec using the two earphone output channels. The booster amplifier for PFH uses the same codec output channel as the external audio. The codec has internal switches for selecting which input or output is used. It also has microphone amplifier with programmable gain and earphone attenuator with programmable attenuation. Input/output selection and amplification/attenuation setting can be done using codec registers. The registers are controlled by the MCU.

Handportable microphone (MICN, MICP) and PHF microphone (PHFMICN, PHFMICP) are connected directly to the codec‘s differential inputs. There is a bias switch in the AUDIO block, which connects the DC bias voltage for both microphones (electret type) when a call is activated. The external microphone signal (EXTMIC) is connected single–ended to the third microphone input channel. There is 21 dB attenuation in the external microphone line before the codec to prevent clipping.

The handportable’s earphone (EARN, EARP) is connected directly to one of the two differential output channels. The output can drive directly a 32 Ω load. The external audio signal (EXTEAR) is connected single–ended to the other output channel. This output is also connected to the input of the Personal Hands–Free booster amplifier. The booster is disabled by MCU when an external audio accessory is used. In PHF mode, the booster is enabled and its differential output is fed to the PHF speaker (PHFEARN, PHFEARP). The load impedance of the PHF speaker is 8 Ω.

Inside the codec, the currently selected microphone signal is routed to the microphone amplifier. After that it is fed to the bandpass filter and then to the A/D converter. After the conversion the digital speech is sent to the DSP in PCM format.

Digital downlink signal from the DSP is fed to the D/A converted. After the converter there is low pass filter and attenuator before the earphone output. All these are inside the codec. The ASIC generates the 512 kHz and 8 kHz clocks for the codec and data transmission between the codec and the DSP.

The audio codec communicates with the DSP (digital speech) through an SIO (signals: PCMIN, SYNC, CODEC_CLK and PCMOUT).The MCU controls the audio codec function through a separate serial bus (signals: PCMCDO, PCMCDI, PCMCLK and XSELPCMC). The PHF power amplifier can be enabled or disabled using the AMP_PWR signal from the MCU. The power amplifier is enabled only when needed due to power consumption reasons.

The codec generates DTMF tones (key beeps) to the earphone and in PHF mode to the PHF speaker. When an external audio accessory is used, the DTMF tones are directed to the external audio output. In handportable and PHF modes the codec generates ringing tones and also some warning tones to the PHF speaker. In external HF mode they are driven to the external speaker line. Some tones come also from the network.

One codec output pin is used to switch on/off the microphone bias circuit. Both microphones are biased simultaneously regardless of which one is actually used.

External microphone line is used also to detect if the junction box is connected to the bottom connector. Microphone signal is therefore low–pass filtered and routed to the MCU A/D converter named as the JCONN signal.

Also external earphone signal is multiplexed. 100 kohm pull down resistor is used to turn power on to the HF accessories.

Main components

– Audio codec ST5090

  Contains e.g. PCM codec, audio routing switches, 3 differential microphone input channels, 2 differential earpiece output channels, ringing tone and DTMF generators. Physically the codec is inside MCM2.

– Power amplifier LM4861 (N400)

  Used as the booster amplifier for Personal Hands–Free.

– Transistors BC859C (V380) and BC849C (V381)

  Used for implementing the microphone bias switch.

ASIC

Introduction

The ASIC takes care of the following functions:

– interface between MCU and UIF
– interface between MCU, DSP and RFI
– hardware accelerator functions to DSP
– clock generation and disable/enable
– RF controls
– UIF interface
– Timers
– MBUS or RBUS activity detection
– SIM interface

Physically the D2CA ASIC is located in MCM2. The VCXO clock buffer and SIM power switch are assembled on CMT motherboard.

Technical specification

Table 36. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL1	Logic supply voltage. Max 150 mA.	PWRU
IOX	I/O enable. Indicates access to DSP I/O address space.	DSPU
RWX	Read/WriteX	DSPU
WSTROBEX	MCU's write strobe	CTRLU
RSTROBEX	MCU's read strobe	CTRLU
RFC	Reference clock from VCXO (26 MHz)	RF
XRES	Master reset	PWRU
DSPAD(16:0)	DSP's address bus and control signals	DSPU
MCUAD(19:16,4:0)	MCU's address bus	CTRLU
DAX	Data acknowledge	RFI
MRBUSDET	MBUS/RBUS activity detection	CTRLU
DBUSDET	DBUS activity detection	DSPU

Table 37. External Signals and Connections, Outputs

Signal Name	Signal description	To
INT0, INT1	Interrupts for DSP	DSPU
NMI	Not maskable interrupt request	CTRLU
IRQX	Interrupt request	CTRLU
RESETX	Master (power up) reset	CTRLU, RFI
DSP1RSTX	Reset for the DSP	DSPU
SIMRESET	Reset for the SIM	SIMFLEX conn
WRX	Write strobe	RFI
RDX	Read strobe	RFI
RFIAD(3:0)	RFI address bus	RFI
SCLK	Synthesizer load clock	RF
SDATA	Synthesizer load data	RF
SENA1	UHF and VHF PLL enable	RF
RXPWR	RX circuitry power enable	RF
TXPWR	TX circuitry power enable	RF
SYNTHPWR	Synthesizer circuitry power enable	RF
TXP	Transmitter power control enable	RF
MCUCLK	Main clock for MCU (26 MHz)	CTRLU

Table 37. External Signals and Connections, Outputs (continued)

Signal Name	Signal description	To
DSPCLKEN	DSP clock circuit enable	DSPU
RFICLK	RFI master clock (13 MHz)	RFI
RFI2CLK	RFI sleep clock (135.4 kHz)	RFI
CODEC_CLK	PCM data clock (512 kHz)	DSPU, AUDIO
PCMDATRCLKX	Inverted PCM data clock (512 kHz) used as input clock for Codec and DBUS interface	DSPU
SYNC	Bit sync clock (8 kHz)	AUDIO
PCMCOSYCLKX	Bit sync clock (8 kHz), inverted	DSPU
DCLK	DBUS data clock (512 kHz)	DSPU
DSYNC	DBUS bit sync clock (8 kHz)	DSPU
SIMCLK	SIM data clock (3.25/1.625 MHz)	SIMFLEX Conn.
VSIM	SIM power control	SIMFLEX Conn.
COL(3:0)	Lines for keyboard column write	B2B Conn.

Table 38. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
DSPDA(15:0)	DSP's 16–bit data bus	DSPU
MCUDA(15:8)	MCU's 8–bit data bus	CTRLU
RFIDA(11:0)	RFI's 12–bit data bus	RFI
UIF(6:0)	LCD–controller control and keyboard read bus	B2B Conn.
SIMDATA	Serial data from/to SIM	SIMFLEX Conn.

Block description

PSL+ supplies the reset to the ASIC at power up. The ASIC starts the clocks to the DSP and the MCU. MCU and RFI reset is released after 256 13 MHz clock cycles. DSP reset release time from DSP clock activation can be selected from 0 to 255 13MHz clock cycles. In our case 255 is selected. SIM reset release time is according to GSM SIM specifications.

The RFC buffer buffers the 26 MHz clock from theVCXO to the ASIC. In the ASIC the clock is further buffered and delivered to MCU. The clock is also divided and delivered to RFI and SIM. ASIC also generates main and sync clocks for audio codec, DSP's SIOs and DBUS. The clock outputs can be disabled in order to save current when the clock is not needed. Also the 60.2 MHz DSP oscillator can be disabled by the ASIC.

Interface to the MCU is done with 8 bit data bus, 5 bit lower address bus, 4 bit upper address bus, RSTROBEX, WSTROBEX, IRQX and NMI. ASIC is in the same memory space as MCU memories. There is also MBUS/RBUS detector and netfree counter on the ASIC. Netfree interrupt IRQX occurs if no activity is detected in MBUS in about 3 ms. ***Note**: This netfree counter cannot be used in the CMT because RBUS data is seen at the same pin.* NMI is used to wake up the MCU from sleep mode.

MCU and DSP communicate through ASIC. ASIC has an MCU mailbox and a DSP mailbox. MCU writes data to DSP mailbox where DSP can only read the incoming data. In MCU mailbox the data transfer direction is the opposite. The size of the mailbox is 64 * 8 bit.

MCU and User Interface (keyboard and display) communication is controlled through the ASIC. COL(3:0) are used as column lines in keyboard. UIF(5:0) are used as row lines They are also multiplexed with display driver control signals.
When a key is pressed the ASIC gets a reset from row and starts scanning. One column at the time is written to low and rows are used to read which key it was. Row lines and UIF6 are used for display driver control. UIF(3:0) are used as 4 bit parallel data bus for the LCD driver. UIF4 is used as read/write strobe, UIF5 to select data or instruction register and UIF6 as enable strobe.

The SIM interface is the electrical interface between the SIM (the smart card used in the GSM and PCN applications) and the MCU via the ASIC. ASIC converts the serial data received from the SIM to parallel data for MCU and converts parallel data from MCU to serial mode for the card. The SIM interface also takes care of the power up and down procedure to the card in addition to frame and parity error checking. The communication between card and ASIC is asyncronous and half duplex.Four signals are used between the ASIC and the SIM card: SIMDATA, SIMCLK,SIMRESET and VSIM. The nominal clock frequency is 3.25 MHz. When there is no data transfer between the SIM card and the CMT the clock can be reduced to 1.625 MHz. Some SIM cards also allow the clock to be stopped in that mode. Supply voltage VSIM can be switched off by the ASIC. The supply voltage range is 4.65–4.95 V. The card detect input of the ASIC is connected to BTYPE pin and when the battery is removed the ASIC will drive the SIM down.

The interface to the DSP is done using 6 bit address bus, 16 bit data bus, IOX and RWX lines. Data bus is latched using IOX, address bus is not. The ASIC also generates interrupt INT0 when an edge occurs in DBUS line (if the mask bit is off). INT1 is used as RX interrupt and as MFI modulator interrupt to the DSP.

Viterbi is used to perform GSM/PCN convolutional decoding and bit detection according to the Viterbi algorithm. It can be controlled and accessed thoroughly by the DSP.

Coder is used to perform block encoding, decoding, and ciphering according to GSM algorithms A5 and A5/2.

The ASIC takes care of the interface between the DSP and the RFI: TX modulator, RX filter, TX and RX sample buffers and controlling state machine. The interface to RFI is done using 12 bit data bus, 4 bit address bus, RDX and WRX. There is also data acknowledge (DAX) signal from RFI to ASIC. Also in this block is the serial RF synthesizer interface (SCLK, SDAT, SENA1) and the digital RF control signals (RXPWR, TXPWR, TXP, SYNTHPWR)

Main components

– D2CA ASIC, physically in MCM2

– 2 x TC7S00F (D300,D301) NAND gate

Inverter buffer stage is used for converting the low–level VCXO clock to valid logic levels.

– Transistors BC848W (V330) and BCW30 (V331)

The SIM power switch.

RFI

Introduction

The RFI block consists of the RFI ASIC and its reference voltage generator. This block is an interface between the RF and baseband sections. The RFI block has the following functions:

– IF receiving and A/D conversion

– I/Q separation

– I– and Q–transmit and D/A conversion

– AFC D/A conversion

– TXC D/A conversion (burst template)

– analog AGC and digital LNA gain switch

Technical specification

Table 39. External Signals and Connections, Inputs

Signal Name	Signal description	From
VL1	Logic supply voltage. Max 150 mA.	PWRU
VA2	Analog supply voltage. Max 80 mA.	PWRU
RESETX	Master (power up) reset	PWRU
RFIAD(3:0)	RFI address bus	ASIC
RDX	Read strobe	ASIC
WRX	Write strobe	ASIC
RFICLK	RFI master clock	ASIC
RFI2CLK	RFI sleep clock	ASIC
RXQ	RX quadrature signal	RF
RXI	RX in–phase signal	RF

Table 40. External Signals and Connections, Outputs

Signal Name	Signal description	To
DAX	Data acknowledge	ASIC
AFC	Automatic frequency control voltage	RF
TXC	TX transmit power control voltage / RX AGC voltage	RF
TXQP,TXQN	differential TX quadrature signal	RF
TXIP,TXIN	differential TX in–phase signal	RF
PDATA0	LNA gain reduction	RF

Table 41. External Signals and Connections, Bidirectional

Signal Name	Signal description	To/From
RFIDA(11:0)	12–bit data bus	ASIC

Block description

The RFI provides A/D conversion of the in–phase (RXI) and quadrature (RXQ) signals in receive path. It has 12 bit A/D converters and the output sample rate is 541.667 kHz.

Analog transmit path includes 8 bit D/A converters to generate the in–phase (TXI) and quadrature (TXQ) signals. RFI has differential outputs for TXI and TXQ. The sample rate is 1.0833 MHz.

There is an 11 bit D/A converter for automatic frequency correction (AFC). The sample rate is 1.3542 kHz.

Power ramp (TXC) is done with 10 bit D/A converter. The sample frequency is 1.0833 MHz. This converter is also used for AGC during receive slots.

The PDATA0 signal is used for LNA gain reduction in strong field conditions. The rest of the AGC control is analog. The analog AGC (used in receive) is multiplexed with the TXC signal (used in transmit).

The RFI has 12 bit data bus to the ASIC. The registers in the RFI are accessed using 4 address bits. Control and clock signals are coming from the ASIC.

The RFI has external 4.096 V voltage reference.

Main components

– RFI ASIC, physically in MCM2

– 4.096 V external voltage reference LM4040 (V420)

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